ABSTRACT

The invention controls maximum average power dissipation by stalling high power instructions through the pipeline of a pipelined processor. A power dissipation controller stalls the high power instructions in order to control the processor's maximum average power dissipation. Preferably, the controller is modeled after a capacitive system with a constant output rate and a throttled input rate: the output rate represents the steady state maximum average power dissipation; while the input rate is stalled based upon current capacity, representing thermal response time. At start-up, the capacity is initialized. Yet for each high power instruction, the capacity increases by a weighted value. Each clock capacity is also decreased by a variable output rate. In particular, a low power operation is inserted to the stage execution circuit where the stall is desired, creating a low power state for that circuit. This stall effectively creates a "hole" at that pipeline stage, thus temporarily reducing power dissipation. The invention takes advantage of the fact that the presence of an instruction at any stage execution circuit dissipates power and that the absence (i.e., a "hole") of an instruction at any stage dissipates less power. By controlling where and when a hole occurs within the pipeline, the maximum average power dissipation of the processor is controlled.